TO: All Vancouver Packet Terminal Node Controller Users

From: Amateur Radio Research and Development (AMRAD)
and Terry Fox, WB4JFI

Subject: New Life for an Old Friend

The Amateur Radio Research and Development Corporation, AMRAD (originators of the now popular AX.25 Level 2 protocol) is pleased to announce that it is now possible to expand the original Vancouver Terminal Node Controller board's memory without raising an X-Acto knife! AMRAD President Terry Fox, WB4JFI has designed a daughter board that plugs into an unmodified VADCG TNC and expand the TNC memory from 4 kilobytes each of EPROM and RAM to up to 32 kilobytes of each. In addition, three software programmable timers are also provided. One timer is used to provide the clock for the 8273 (HDLC chip) on the VADCG TNC. The other two timers are used to generate timed interrupts for the VADCG TNC (8085). One timer generates maskable interrupts (INTR pin), while the other timer generates non-maskable interrupts (TRAP pin). These timers can be used to give the programmer a more accurate method of controlling protocol functions.

In addition, there are several 16 pin sockets, one 24 pin socket, and a general kludge area provided for the user. This allows for additions such as transmitter time-out timers, or modems.

EPROM Description

There are four EPROM sockets provided. The sockets are spaced so that Zero Insertion Force (ZIF) sockets can be used if frequent EPROM changing is expected. The board uses the present memory decoder chip (relocated onto the daughter board), with a jumper area used to define what type of EPROM is being used. The board comes jumpered for 2732 type EPROMs, but 2716, and 2764 types are also usable. JEDEC 28 pin socket layout is used.

RAM Description

As in the EPROM area above, the RAM sockets also conform to the 28 pin Jedec layout. The four RAM sockets will accept either 2K devices (6116 type), or 8K devices (either static or psuedo-static that are Intel 2186 compatible. The RAM address decoder is similar to the EPROM decoder, except that the jumper is set to 6116 type devices. RAM address mapping is set to begin at 8000 hex, to conform with older mods to the Vancouver TNC.

Timer Description

In addition to the new memory used on the daughter board, an Intel 8253 timer is implemented. This device has three independant software controllable timers, each with a sixteen bit divider. The old hardware baud-rate divider (CD4024) for the HDLC channel has been moved up to the daughter board, and acts as a pre-divider to the 8253 chip. Each of the 8253 timer's clock inputs are jumperable to one of the outputs of the CD4024, allowing timed interrupts over a large variation of times. Timer 0 is now used to generate the clock for the HDLC channel. Timer 1 is normally jumpered to the 8085 trap pin on the Vancouver TNC, which is non-maskable. Timer 2 is normally jumpered to the 8085 INTR pin. The INTR pin creates an interrupt that is maskable by the CPU. The two-interrupt system allows versatile programming techniques to be used, along with better error recovery.

Daughter Board Installation

The daughter board is about 4.5 by 9 inches in size. Installation requires no wire jumpers between the two boards, and may not require any trace cutting on the Vancouver board. If timed interrupts are to be used from the daughter board timer chip, two traces must be cut on the VADCG TNC, since both the Trap and INTR pins are normally shorted to ground. NO OTHER TRACES ARE CUT!! The only other requirement is that several IC sockets on the Vancouver TNC must be capable of accepting large pins.

Connections made between the Vancouver board and the AMRAD daughter board are made through four wirewrap sockets that plug into the Vancouver board instead of the IC's that would otherwise be there. These four IC's are:

U1 8085 CPU chip
U18 2708 EPROM, upper left corner

U9 74LS138 I/O port decoder
U11 CD-4024 Baud rate divider.

All power and signals are sent between the two boards using these four sockets. It should be noted that since 2708 EPROMs are no longer being used, the minus five volt supply can be eliminated.

The first step (after making sure that the TNC board operates properly without modification) is to remove several of the Integrated Circuits from the VADCG TNC. They are:

U1 8085 CPU
U7 74LS00 Memory decoder logic.
U8 74LS138 Memory decoder.
U9 74LS138 I/O port decoder.
U11 CD-4024 Baud-rate divider.
U15-U18 2708 EPROM chips.
U19-U26 2114 RAM chips.

Now, check out the jumpers and alter them as required for the configuration required.

The next installation step is to place the daughter board over the Vancouver board so that the long wire-wrap socket pins extend into the IC sockets U1, U9, U11, and U18. Once the pins line up properly, gently press the wire-wrap socket pins into the VADCG IC sockets. Make sure that all pins line up properly, and none are bent.

It is possible that the present IC sockets on the Vancouver TNC will not accept the larger pins of the wire-wrap sockets on the daughter board. If this happens, the IC offending sockets must be replaced in order to use the daughter board. This isn't as hard as it seems (I had to do it for the prototype board). Be careful, and use a good solder-sucker when removing the old sockets.

Now plug U1 (8085) and U9 (74LS138) into their wire-wrap sockets on the daughter board. Place some tape over U18 and U11, so no ICs are accidentally plugged into them (they are only used to gain access to certain lines on the Vancouver board).

Next, plug in the rest of the IC's and test the board out.

Parts Required

The daughter board has been designed to require a minimum of additional components, while maintaining a high degree of operation. Actually, there are only two additional support IC's required (in addition to the EPROMs and RAMs of course).

1 AMRAD Daughter Board.
1 74LS138 decoder IC.
1 Intel 8253 interval timer IC.
4 EPROMS, 2732 nominal (2716, 2764 optionally).
4 RAMs, 6116 nominal (8K parts optional).
1 40 pin wire-wrap socket.
1 24 pin wire-wrap socket.
1 16 pin wire-wrap socket.
1 14 pin wire-wrap socket.
8 28 pin solder-tail sockets.
1 24 pin solder-tail socket.
2 16 pin solder-tail sockets.
2 14 pin solder-tail sockets.
2 14 pin solder-tail sockets (optional).
2 14 pin DIP headers (optional).
1 100 UF 10 volt Electrolytic capacitor.
5 .1 UF 50 volt disc ceramic capacitors.

End of Parts List

Well, that's a brief description of the AMRAD Vancouver Daughter Board. The initial run of boards are being made now, watch for more information here, or in the AMRAD Newsletter (yes, it is still around, with a new editor, Deborah Borden). Or write to:

AMRAD, PO Drawer 6148, McLean Virginia, 22106-6148, or:

Terry Fox, WB4JFI, 1819 Anderson Rd., Falls Church VA 22043

Also, watch for a completely new set of Assembly-language code from AMRAD for the Vancouver board, AMRAD PAD (coming out soon), or most any other 8080, 8085, or Z80 based computer (including CP/M, S100, and Xerox 820 systems). NETWARE (TM) is written in modular form,

similar to Ward Christensen's Computerized Bulletin Board System (CBBS)TM software, with hooks and modules coming for AX.25 Level 3 (networking).

Thank you for your time, and happy framing!!!

Terry Fox, WB4JFI